Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **VCC1**
2. **Q1**
3. **N. Q1**
4. **R1**
5. **S1**
6. **N. CE1**
7. **D1**
8. **VEE**
9. **C**
10. **D2**
11. **N. CE2**
12. **S2**
13. **R2**
14. **N. Q2**
15. **Q2**
16. **VCC2**

**.058”**

****

**.070”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .058” X .070” DATE: 11/15/21**

**MFG: MOTOROLA THICKNESS .015” P/N: MCC10131**

**DG 10.1.2**

#### Rev B, 7/1